REMARKS

Claims 1-42 are pending in this application.

Claims 1-42 stand rejected under 35 U.S.C. 102(e) as being anticipated by Jones et al. (U.S. Patent No. 6,555,858) ("Jones"). This rejection is respectfully traversed.

The claimed invention relates to a method of forming a magnetic random access memory. As such, independent claim 1 recites a "method of forming a magnetic random access memory" by *inter alia* "forming a plurality of spaced apart magnetic memory element stacks over said plurality of first conductive layers, wherein each of said magnetic memory element stacks is formed by the steps of forming a first magnetic layer over a corresponding first conductive layer and forming a second magnetic layer over said first magnetic layer, said second magnetic layer having an associated top conductive layer." Independent claim 1 also recites "forming an insulating material over and in between said spaced apart magnetic memory element stacks." Independent claim 1 further recites "removing at least a portion of said insulating material over at least one of said memory element stacks to expose the top conductive layer of said at least one memory element stack."

Independent claim 21 recites a "method of forming a magnetic random access memory" by *inter alia* "forming a plurality of spaced apart magnetic memory element stacks over said plurality of first conductive layers, wherein each of said magnetic memory element stacks is formed by the steps of forming a first magnetic layer over a corresponding first conductive layer and forming a second magnetic layer over said first magnetic layer, said second magnetic layer having an associated top conductive layer." Independent claim 21 also recites "forming an insulating material over and in between said spaced apart magnetic memory element stacks" and "removing at least a portion of said insulating material to expose upper surfaces of a plurality of said memory element stacks."

Jones relates to a "self-aligned magnetic clad bit line structure (274) for a magnetic memory element (240a)." (Abstract; Figure 13). Jones teaches that "the self-

aligned magnetic clad bit line structure (274) extends within a trench (258) and includes a conductive material (250), magnetic cladding sidewalls (262) and a magnetic cladding cap (252)." (Abstract; Figure 13). Jones also teaches that "[t]he magnetic cladding sidewalls (262) at least partially surround the conductive material (264) and the magnetic cladding cap (252) is substantially recessed within the trench with respect to the top of the trench." (Abstract; Figure 13).

Jones fails to disclose all limitations of independent claims 1 and 21. Jones fails to teach or suggest "forming a plurality of spaced apart magnetic memory element stacks . . . by the steps of forming a first magnetic layer over a corresponding first conductive layer and forming a second magnetic layer over said first magnetic layer, *said second magnetic layer having an associated top conductive layer*," and "forming an insulating material *over and in between* said spaced apart magnetic memory element stacks," as independent claims 1 and 21 recite. Jones teaches that "bit line structure 274 electrically connects to the magnetic memory elements 240a and 240b" and that "bit line structure 274 is a magnetically clad bit line structure that includes conductive material 250 and a self-aligned magnetic cladding capping layer 252." (Col. 6, lines 39-43). Jones also teaches that "magnetic memory element layers 234, 236 and 238 are deposited over the conductive layer 232." (col. 5, lines 31-32). Jones is silent, however, about "forming a first magnetic layer over a corresponding first conductive layer and forming a second magnetic layer over said first magnetic layer, *said second magnetic layer having an associated top conductive layer*," as independent claims 1 and 21 recite. In Jones, magnetic memory element layer 236, which would arguably correspond to the second magnetic layer of the claimed invention, does not have "an associated top conductive layer," as recited in independent claims 1 and 21.

Jones also fails to disclose "forming an insulating material *over and in between* said spaced apart magnetic memory element stacks," as independent claims 1 and 21 recite. Jones teaches that passivation layer 254 is formed "[o]verlying the bit line structure 274." (Col. 6, lines 43-44). However, as shown in Figures 13 and 14 of Jones, passivation layer

254 is not formed "over and in between" magnetic memory element layers 234, 236 and 238.

Jones also fails to teach or suggest "removing at least a portion of said insulating material over at least one of said memory element stacks to expose the top conductive layer of said at least one memory element stack," as independent claim 1 recites, or "removing at least a portion of said insulating material to expose upper surfaces of a plurality of said memory element stacks," as independent claim 21 recites. As noted above, Jones teaches the formation of passivation layer 254 over the self-aligned magnetic clad bit line structure (274) for a magnetic memory element (240a); however, Jones does not teach "removing of at least a portion of said insulating material [passivation layer 254]" to expose upper surfaces of top conductive layers of said memory element stacks, as in the claimed invention. For at least these reasons, Jones fails to disclose all limitations of claims 1-42, and withdrawal of the rejection of these claims is respectfully requested.

Applicant notes that the assertion of the Office Action that "figures 1-15 and related text [of Jones] discloses forming several spaced apart first conductive layers 226 over an insulating layer 218 over a substrate 200; forming several spaced apart magnetic memory element stacks 228 over the several first conductive layers" is incorrect. (Office Action at 2). Layer 228 of Jones is a "conductive layer" which is "deposited over the layer of high-permeability magnetic material 226 to substantially fill the trenches 225 and contact window openings 227" (col. 4, lines 59-62; Figure 3), and not a "magnetic memory element stack," as the Office Action mistakenly asserts.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: October 17, 2003

Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
Gabriela I. Coman
Registration No.: 50,515
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant